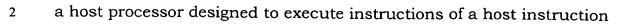
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٠.	1	Claim 4. A system for protecting memory from being written as
	2	claimed in Claim 1 in which the hardware means comprises:
	3	a look-aside buffer including a plurality of storage locations for
	4	virtual addresses and associated physical addresses, and
	5	a storage position in each storage location of the translation look
	6	aside buffer; and
7	~ 7	in which the software means for protecting against writing the memory
l	8	address invalidates translations associated with the memory address
	103	Claim 5. A system for protecting memory from being written as
}	\mathcal{L}_{2}^{\prime}	claimed in Claim 1 in which the software means for protecting against
O	2	writing the memory address removes translations associated with the
	3	writing the memory address removes translations associated with the
	4	memory address.
	4	memory address.
	1	memory address. Claim 6. A system for protecting memory from being written as
	1 2	memory address. Claim 6. A system for protecting memory from being written as claimed in Claim 1 in which the hardware means comprises:
	1 2	memory address. Claim 6. A system for protecting memory from being written as claimed in Claim 1 in which the hardware means comprises: a look-aside buffer including a plurality of storage locations for
	4 1 2 3 4	memory address. Claim 6. A system for protecting memory from being written as claimed in Claim 1 in which the hardware means comprises: a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses, and
	4 1 2 3 4	memory address. Claim 6. A system for protecting memory from being written as claimed in Claim 1 in which the hardware means comprises: a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses, and a storage position in each storage location of the translation look
	4 1 2 3 4 5 6	memory address. Claim 6. A system for protecting memory from being written as claimed in Claim 1 in which the hardware means comprises: a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses, and a storage position in each storage location of the translation look aside buffer; and
	4 1 2 3 4 5 6	memory address. Claim 6. A system for protecting memory from being written as claimed in Claim 1 in which the hardware means comprises: a look-aside buffer including a plurality of storage locations for virtual addresses and associated physical addresses, and a storage position in each storage location of the translation look aside buffer; and in which the software means for protecting against writing the memory



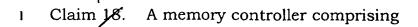
- 3 set,
- software for translating instructions from a target instruction set to
- instructions of the host instruction set,
- 6 memory for storing target instructions from a program being translated,
- a translation buffer for storing host instructions translated from target
- 8 instructions for execution, and
- 9 hardware means for generating an exception to a write access to a target
- address storing a target instruction which has been translated to a host
- 11 instruction.
 - Claim 8. A computer system as claimed in Claim 7 in which the
 - hardware means for generating an exception comprises a translation
- look-aside buffer including a plurality of storage locations for virtual and
- 4 physical addresses of recently accessed memory, each of the storage
- location including a storage position for indicating that an instruction at
- a target address has been translated to a host instruction.
- Claim 9. A computer system as claimed in Claim 7 further comprising
- 2 software means responding to an exception to a write access to a target
- address storing a target instruction which has been translated to a host
- 4 instruction for protecting against writing the memory address until it has
- been assured that translations associated with the memory address will
- 6 not be utilized before being updated.



- Claim 10. A computer system as claimed in Claim 9 in which the
- software means responding to an exception to a write access comprises
- software means invalidating translations associated with the memory
- 4 address.
- Claim 11. A computer system as claimed in Claim 9 in which the
- software means responding to an exception to a write access comprises
- 3 software means removing translations associated with the memory
- 4 address.
- Claim 12. A method of responding to an attempt to write a memory
- 2 address including a target instruction which has been translated to a
- host instruction for execution by a host processor including the steps of:
- 4 marking a memory address including a target instruction which has
- been translated to a host instruction,
- 6 detecting a memory address which has been marked when an attempt is
- 7 made to write to the memory address, and
- responding to the detection of a memory address which has been marked
- by protecting a target instruction at the memory address until it has
- been assured that translations associated with the memory address will
- not be utilized before being updated.
- Claim 13. A method as claimed in Claim 1/2 in which the step of
- 2 marking a memory address including a target instruction which has
- been translated to a host instruction comprises storing an indication that
- a target address has been translated in a memory location of a

- translation look-aside buffer with a physical address of the target
- 6 instruction.
- 1 Claim 14. A method as claimed in Claim 12 in which the step of
- responding to the detection of a memory address which has been marked
- by protecting a target instruction at the memory address until it has
- been assured that translations associated with the memory address will
- not be utilized before being updated comprises the steps of:
- generating an exception in response to the detection of a memory
- 7 address which has been marked, and
- responding to the exception by invalidating translations associated with
- the memory address before writing the memory address.
- Claim 15. A microprocessor comprising:
- a host processor capable of executing a first instruction set,
- code morphing software for translating programs written for a target
- processor having a second different instruction set into instructions of
- the first instruction set for execution by the host processor, and
- a memory controller comprising
- an address translation buffer including a plurality of storage
- locations in which recently accessed virtual target addresses and
- 9 physical memory addresses represented by the virtual target
- addresses are to be recorded,

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- 2 an address translation buffer including a plurality of storage locations in
- which recently accessed virtual addresses and physical addresses
- 4 represented by the virtual addresses are to be recorded,
- 5 each of the storage locations including means for indicating
- 6 whether a physical address stores an instruction of a target
- 7 instruction set which has been translated to an instruction of a
- 8 host instruction set; and
- 9 means for detecting an indication in a storage location to prevent a write
- access of to the physical address and for indicating a subsequent
- operation before accessing the address.
- Claim 19. A memory controller as claimed in Claim 18 in which the
- 2 / means for detecting an indication in a storage location to prevent a write
- access of to the physical address and for indicating a subsequent
- 4 operation before accessing the address comprises
- 5 means for generating an exception in response to detection of an
- 6 indication, and
- 7 means for responding to the exception to indicate a subsequent
- 8 operation to be taken with respect to the translated host instruction
- 9 before accessing the address.
- 1 Claim 26. A memory controller as claimed in Claim 18 in which the
- 2 means for indicating comprises a storage position in a storage location.

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- Claim 1. A system for protecting memory from being written in a computer which includes a host processor designed to execute instructions of a host instruction set and software for translating instructions from a target instruction set to instructions of the host
- instruction set comprising:
- 6 hardware means for indicating whether a memory address stores a target
- instruction which has been translated to host instructions, and
- software means responding to an indication that a memory address
- stores a target instruction which has been translated to host instructions
- of for protecting against writing the memory address until it has been
 - assured that translations associated with the memory address will not be
 - utilized before being updated once the memory address has been written.
 - Claim 2. A system for protecting memory from being written as
 - claimed in Claim 1 in which the hardware means comprises:
 - a look-aside buffer including a plurality of storage locations for virtual
 - addresses and a sociated physical addresses, and
 - a storage position in each storage location of the translation look aside
 - 6 buffer.
 - Claim 3. / A system for protecting memory from being written as
 - claimed in Claim 1 in which the software means for protecting against
 - writing/the memory address invalidates translations associated with the
 - 4 memory address.

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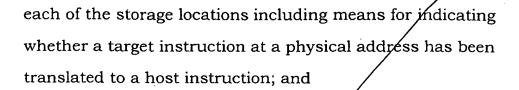
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means for responding to a write access of an address in a storage location of the address translation buffer in which the means for indicating indicates that a target instruction at a physical address has been translated to a host instruction for protecting against writing the memory address until it has been assured that translations associated with the memory address will not be utilized before being updated.

- Claim 16. A microprocessor as claimed in Claim 15 in which the means
- for responding to a write access of an address in a storage location of the
- address translation buffer in which the means for indicating indicates
- 4 that a target instruction/at a physical address has been translated to a
- 5 host instruction for protecting against writing the memory address
- 6 comprises
- 7 means for generating an exception in response to a detection of an
- 8 indication, and
- 9 means for responding to the exception to indicate a subsequent
- operation to be taken before accessing the memory address.
- Claim 17/ A microprocessor as claimed in Claim 16 in which the means
- 2 for indicating whether a target instruction at a physical address has been
- trans/ated to a host instruction comprises a storage position in a storage
- 4 location.

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